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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/254,939	03/17/99	MIURA H	500.36904X00

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ANTONELLI TERRY STOUT & KRAUS
1300 NORTH SEVENTEENTH STREET
SUITE 1800
ARLINGTON VA 22209

EXAMINER	
MAI, A	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 01/26/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/254,939	MIURA ET AL.	
	Examiner	Art Unit	
	Anh D. Mai	2814	

-- Th MAILING DATE of this communic tion appears on the cov r sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 November 2000* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 9-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 9-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☒ The proposed drawing correction filed on *09 November 2000* is: a)☒ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claims 10-14 and 15-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 10 recites: *increasing a curvature* of an upper end portion of said trench (line 13).

Similarly, claim 15 recites: *increase a curvature* of the semiconductor substrate (line 10).

Since a curvature has not been created, therefore "increasing" or "increase" a non-exist entity is indefinite.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 1 is rejected under 35 U.S.C. 102(b) as being clearly anticipated by Ooka (U.S. Patent No. 4,740,480).

Ooka teaches a method of fabricating a semiconductor device as claimed including:

(a) forming an oxidation prevention film (13) on a circuit formation surface of a semiconductor substrate (11);

(b) forming a trench (15) having a desired depth at a predetermined position of the circuit formation surface of the semiconductor substrate;

(c) oxidizing the trench portion formed in the semiconductor substrate, exposed in the trench;

(d) burying a buried insulating film (17) into the trench so oxidized;

(e) after burying the buried insulating film, oxidizing the semiconductor substrate;

(f) removing the buried insulating film formed on said oxidation prevention film (13);

(g) eliminating the oxidation prevention film (13) formed on the semiconductor substrate; and

(h) after eliminating the oxidation prevention film, forming a gate oxidation film (19). (See Figs. 2A-I, col. 5, l. 1-col. 6, l. 33).

3. Claim 9 is rejected under 35 U.S.C. 102(b) as being clearly anticipated by Ooka '480.

Ooka teaches a method of fabricating a semiconductor device as claimed including:

(a) forming an oxidation prevention film (13) on a circuit formation surface of a semiconductor substrate (11);

(b) forming trench regions (15) in the substrate from the circuit formation surface thereof;

(c) performing a first oxidation to form an oxide film (12') on the trench regions (15);

(d) forming an insulating film (17) inside the oxidized trench regions so as to completely fill them;

(e) performing a second oxidation to selectively oxidize an opening side of the completely filled trench regions in the substrate; and

(h) after performing the second oxidation, forming a gate oxidation film (19). (See Figs. 2A-I, col. 5, l. 1-col. 6, l. 33).

4. Claim 10-13 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Ooka '480.

As best under stood by examiner, Ooka teaches a method of fabricating a semiconductor device as claimed including:

(a) forming an oxidation prevention film (13) on a circuit formation surface of a semiconductor substrate (11);

(b) forming a trench (15) having a desired depth at a predetermined position of the circuit formation surface of the semiconductor substrate;

(c) oxidizing the trench portion formed in the semiconductor substrate, exposed in the trench;

(d) burying a buried insulating film (17) into the trench so oxidized;

(e) after burying the buried insulating film, increasing a curvature of an upper end portion of the trench;

(f) removing the buried insulating film formed on the oxidation prevention film (13); and

(g) removing the oxidation prevention film (13) formed on the circuit formation surface of the semiconductor substrate. (See Figs. 2A-G, col. 5, l. 1-col. 6, l. 33).

With respect to claims 11-13, the second oxidation of Ooka is inherently result in increasing the curvature, forming bird' beak and having an angle as claimed.

5. Claim 15-17 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Ooka '480.

As best under stood by examiner, Ooka teaches a method of fabricating a semiconductor device as claimed including:

(a) forming an oxidation prevention film (13) on a circuit formation surface of a semiconductor substrate (11);

(b) forming a trench (15) having a desired depth at a predetermined position of the circuit formation surface of the semiconductor substrate;

(c) oxidizing the trench portion formed in the semiconductor substrate, exposed in the trench, so as to increase a curvature of the semiconductor substrate of an upper end portion of the trench;

(d) burying a buried insulating film (17) into the trench so oxidized;

(e) removing the buried insulating film formed on the oxidation prevention film (13); and

(g) removing the oxidation prevention film (13) formed on the circuit formation surface of the semiconductor substrate. (See Figs. 2A-G, col. 5, l. 1-col. 6, l. 33).

With respect to claim 16, the oxidizing of trench (15) in the process of Ooka is inherently result in forming a bird's beak at the upper end portion of the trench, so as to increase the curvature.

With respect to claim 17, the oxidizing of Ooka is thermal oxidation, thus, to increase the curvature.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ooka '480 in view of Miyashita et al. (EP. Patent No. 459397).

Ooka teaches a method of fabricating a semiconductor device substantially as claimed including the steps of:

(a) forming an oxidation prevention film (13) on a circuit formation surface of a semiconductor substrate (11);

(c) forming trenches (15) having a predetermined depth;

(d) oxidizing the trench portions formed in the semiconductor substrate, exposed in the trenches;

(e) burying a buried insulating film (17) into the trenches so oxidized;

(f) oxidizing the semiconductor substrate after burying the buried insulating film;

(g) removing the buried insulating film (17') formed on the oxidation prevention film (13);

(h) eliminating the oxidation prevention film (13) formed on the semiconductor substrate; and

(i) after eliminating the oxidation prevention film, forming a gate oxidation film (19). (See Figs. 2A-I, col. 5, l. 1-col. 6, l. 33).

Thus, Ooka is shown to teach all of the features of the claim with the exception of forming a shallow trenches having a radius of curvature prior to forming trenches (15).

However, Miyashita '397 teaches forming shallow trenches (26) having a radius of curvature (27) prior to forming the isolation trench (28) to avoid the concentration of electric field at the corner of the trench thereby preventing lowering the threshold voltage of the MOSFET. (See Figs. 2A-C, col. 2, l. 50-col. 3, l. 12).

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form shallow trench (26) having radius of curvature (27) prior to forming trenches (15) of Ooka '480 as taught by Miyashita '397 to avoid the concentration of electric field at the corner of the trench thereby preventing lowering the threshold voltage of the MOSFET.

With respect to claim 3, the process for forming the shallow trench (26) of Miyashita '397 is carry out by isotropic etching and the step for forming the trench (28) is carry out by anisotropic etching.

7. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fazan et al. (U.S. Patent No. 5,433,794) in view of Perera (U.S. Patent No. 5,786,263).

Fazan teaches a method of fabricating a semiconductor device similar as claimed including the steps of:

(a) forming an oxidation prevention film (3) on a circuit formation surface of a semiconductor substrate (1);

(b) forming trench having a predetermined depth at desired positions of the circuit formation surface of the semiconductor substrate;

(c) oxidizing the trench portions (2A) formed in the semiconductor substrate, exposed in the trench;

(d) burying a buried insulating film (4) into the trenches so oxidized;

(e) removing the buried insulating film formed on the oxidation prevention film; and

(g) removing the oxidation prevention film (3) formed on the circuit formation surface of the semiconductor substrate. (See Figs. 3-6, col. 2, l. 25-col. 3, l. 33).

Thus, Fazan is shown to teach all of the features of the claim with the exception of oxidizing the semiconductor substrate (1) after the buried insulating film (4) formed on the oxidation prevention film is removed and forming gate oxidation film.

However, Perera teaches oxidizing the semiconductor substrate (12) after the buried insulating film (34) formed on the oxidation prevention film is removed and forming gate oxidation film (40). (See col. 4, ll. 9-21).

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to oxidizing the semiconductor substrate (1) of Fazan after the buried insulating film (4) formed on the oxidation prevention film is removed to densify the buried insulating film.

Further, forming the gate oxide after the removal of the oxidation prevention is a well known process sequence in the VLSI technology as shown by Perera.

8. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fazan '794 in view of Miyashita '397 and Perera '263.

Fazan teaches a method of fabricating a semiconductor device as claimed including the steps of:

(a) forming an oxidation prevention film (3) on a circuit formation surface of a semiconductor (1);

(c) forming trenches having a predetermined depth in the semiconductor substrate;

(d) oxidizing the trench portions formed in the semiconductor substrate, exposed in the trench;

(e) burying a buried insulation film (4) into the trenches so oxidized;

(f) removing the buried insulating film formed on the oxidation prevention film (3); and

(h) removing the oxidation prevention film (3) formed on the circuit formation surface of the semiconductor substrate. (See Figs. 3-6, col. 2, l. 25-col. 3, l. 33).

Thus, Fazan is shown to teach all of the features of the claim with the exception of forming a shallow trench having a radius of curvature prior to forming the trench; oxidizing the semiconductor substrate (1) after the buried insulating film (4) formed on the oxidation prevention film (3) is removed and forming gate oxidation film.

However, Miyashita '397 teaches forming shallow trenches (26) having a radius of curvature (27) prior to forming the isolation trench (28) to avoid the concentration of electric field at the corner of the trench thereby preventing lowering the threshold voltage of the MOSFET. (See Figs. 2A-C, col. 2, l. 50-col. 3, l. 12).

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form the shallow trench (26) prior to forming the trench of Fazan '794 as taught by Miyashita '397 to avoid the concentration of electric field at the corner of the trench thereby preventing lowering the threshold voltage of the MOSFET.

Further, Perera teaches oxidizing the semiconductor substrate (12) after the buried insulating film (34) formed on the oxidation prevention film is removed and forming the gate oxide (40). (See col. 4, ll. 9-21).

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to oxidizing the semiconductor substrate (1) of Fazan after the buried insulating film (4) formed on the oxidation prevention film is removed to densify the buried insulating film.

Furthermore, forming the gate oxide after the removal of the oxidation prevention is a well known process sequence in the VLSI technology as shown by Perera.

With respect to claim 6, the process for forming the shallow trench (26) of Miyashita '397 is carry out by isotropic etching and the step for forming the trench (28) is carry out by anisotropic etching.

9. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ooka '480 as applied to claim 10 above, and further in view of Perera '263.

Ooka is shown to teach all of the features of the claim with the exception of performing the second oxidation after the removal of the buried insulating film formed on the oxidation prevention layer.

However, Perera teaches performing a second oxidation following the removal of the buried insulating film formed on the oxidation prevention layer. (See col. 4, ll. 9-21).

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to perform the second oxidation of Ooka after the buried insulating film (4) formed on the oxidation prevention film is removed to shorten the oxidation time, thus, higher through put.

Response to Arguments

10. Applicant's arguments with respect to claims 1-6, 9 and 10 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (703) 305-0575. The examiner can normally be reached on 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

A.M
January 17, 2001

OLIK CHAUDHURI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800